Remarks

The foregoing amendments and these remarks are in response to the Final Office Action dated July 14, 2004.

Prior to addressing the Examiner's rejections on the art, a brief review of applicant's invention is appropriate. The invention relates to a variable conduction device that is coupled to a scanning velocity modulation (SVM) deflection signal generator that includes a single transistor having two signal inputs. For instance, the transistor is operable both as a common emitter amplifier and as an amplifier configured for common base operation. One of the transistor input electrodes (emitter) is responsive to a feedback signal representative of the SVM deflection signal, and the other input electrode (base) is responsive to a control signal. In a first condition, the transistor receives the feedback signal and provides a feedback path for controlling the magnitude of the SVM deflection signal. In a second condition, the control signal causes the transistor to interrupt the feedback path and inhibit generation of the SVM deflection signal by attenuating the input signal fed to the SVM amplifier. Accordingly, the variable conduction device not only controls the magnitude of the SVM deflection signal by means of negative feedback, but in addition turns the deflection signal on or off using just a single transistor, thus controlling the SVM deflection signal at minimum cost.

Claim Rejections on the Art

At the time of the Office Action, claims 1-6 and 8-13 were pending in the application. Claims 1-6 and 8-13 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,072,300 to Anderson ("Anderson"). Anderson provides a circuit for selectively disabling normal SVM circuit operation when an on screen display generator is being used. Importantly, Anderson discloses the use of at least four transistors 65, 118, 133 and 136 for implementation of his SVM solution.

Amended claim 1 and claim 8 each recite a generator of a scanning velocity modulation deflection signal comprising a variable conduction device. As recited in claim 1, the variable conduction device itself comprises a transistor having a first input responsive to a scanning velocity modulation deflection signal

and a second input responsive to a control signal. Similarly, claim 8 recites that the variable conduction device consists of a single transistor having a first terminal responsive to a scanning velocity modulation feedback signal, and a second terminal responsive to a control signal.

Anderson fails to teach or suggest these limitations. In particular, as the Examiner noted on page 5 of the Office Action, in Anderson's circuit the feedback loop and control signal are both applied to the base electrode of transistor 65. However, Anderson's circuit arrangement must also use transistors 133, 136 and 118 to control the SVM deflection signal. Thus, Anderson uses four transistors to implement a task which is advantageously performed by Applicant's invention using a single transistor, namely transistor Q1.

Amended claim 1 further recites that in a first condition the single transistor provides a feedback path for receiving the feedback signal at the first input for controlling a magnitude of the scanning velocity modulation deflection signal. Additionally, claim 1 recites that in a second condition the transistor interrupts the path and substantially inhibits generation of the scanning velocity modulation deflection signal in response to the second input receiving the control signal. Anderson fails to teach or suggest this limitation. As noted, in Anderson's circuit both the control and feedback signals are applied to the same input, i.e. the base of transistor 65.

Claim 9 recites a scanning velocity modulation deflection signal generator, comprising a transistor. Advantageously Applicant's single transistor is arranged to function in different modes of operation. Transistor (Q1) is coupled to the scanning velocity modulation deflection signal generator and is operational as a common base amplifier for a feedback signal coupled for controlling a magnitude of the scanning velocity modulation deflection signal. The transistor is also operational as a common emitter amplifier for interrupting the feedback signal and substantially inhibiting generation of the scanning velocity modulation deflection signal. The Examiner has asserted that this limitation is disclosed by Anderson and presents the operation of transistor 65 to support this assertion.

However, Applicant believes the Examiner may have misunderstood the teachings of Anderson in making the foregoing rejection. Accordingly, it is believed that a brief review of Anderson's circuit will be helpful for assisting the Examiner in recognizing the differences between Anderson's disclosure and the

invention recited in Applicant's claim 9. As noted by the Examiner on page 5 of the Office Action, who asserts that both operations of amplifying the feedback signal and interrupting the feedback signal are met solely by the current source transistor 65. However, in both instances Anderson's transistor 65 operates as a common emitter amplifier. Accordingly, Anderson fails to show or disclose,

a transistor that is operational both as a common base amplifier, for controlling SVM signal magnitude, and in addition,

is operational as a common emitter amplifier for interrupting the feedback signal.

As noted, the failure of Anderson to utilize transistor 65 in both a common base and a common emitter configuration necessitates the use of at least additional transistors 118, 133 and 136 to achieve the functionality that Applicant has achieved with his single transistor Q1. Accordingly, Anderson's circuit is more costly than Applicant's claimed invention and more susceptible to failure due to an increased transistor and component count.

Claims 10 and 12 each recite that the negative feedback signal is representative of power dissipation in a scanning velocity modulation drive amplifier responsive to the scanning velocity modulation deflection signal. The Examiner has asserted that this limitation is met by the base of the transistor 65 being coupled to the collector of transistor 136. However, transistor 136 does not provide a negative feedback signal to transistor 65, and thus the combination of transistors 65 and 136 do not disclose the recited limitation.

Claim 13 recites the scanning velocity modulation deflection signal generator of claim 9, wherein the common emitter amplifier substantially inhibits generation of the scanning velocity modulation deflection signal by attenuating a signal input to the generator. The Examiner asserts that this limitation is met by Anderson's common emitter amplifier 32. Seemingly the Examiner has overlooked that claim 13 is dependent on claim 9. Imparted to claim 13 from claim 9 is the limitation that a single transistor operates as both a common emitter and common base amplifier. In contrast, circuitry 32 which the Examiner has asserted as Anderson's common emitter amplifier actually functions with a plurality of transistors, namely transistors 51, 52 and 65. Furthermore, Anderson teaches, at column 6, line 32, that amplifier 32 is a differential amplifier. In addition at column 6, lines 28 to 35, Anderson describes the operation of differential

amplifier 32 during an OSD, teaching that the current source transistor 65 is controlled. In addition to the different transistor circuit configuration employed by Anderson, Anderson also fails to show or suggest Applicant's recited "attenuating a signal input to said generator".

Thus, Anderson does not disclose a transistor operational as a common emitter amplifier for interrupting the feedback signal and inhibiting generation of the scanning velocity modulation signal by attenuating a signal input to the generator.

Although Anderson's teachings are directed to objectives similar to applicant's, his respective circuit solutions are significantly different. Applicant's novel circuit arrangement using a single transistor to perform dual functions is not shown nor suggested by Anderson and is therefore considered patentable over Anderson's teachings. Applicant respectfully requests the withdrawal of the rejection of claims 1 - 6 and claims 8 - 13.

Respectfully submitted,
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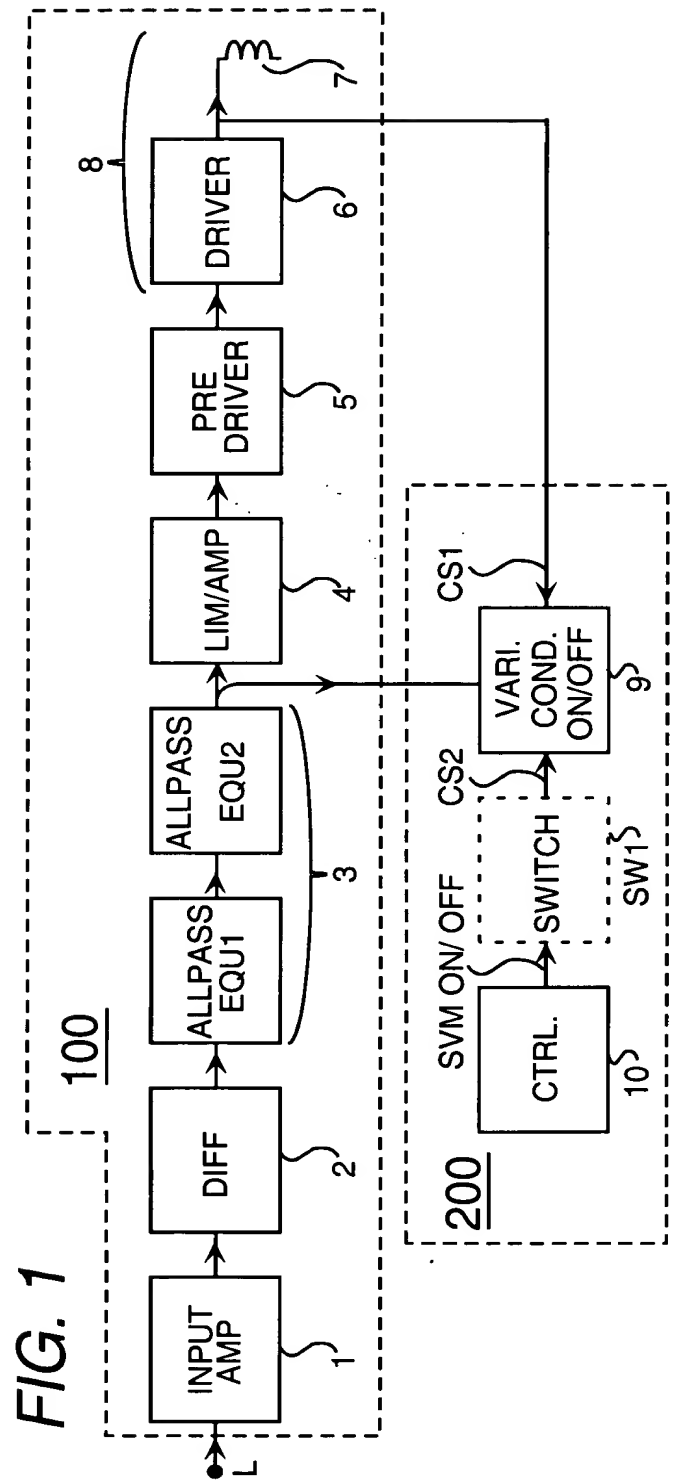
FIG. 1



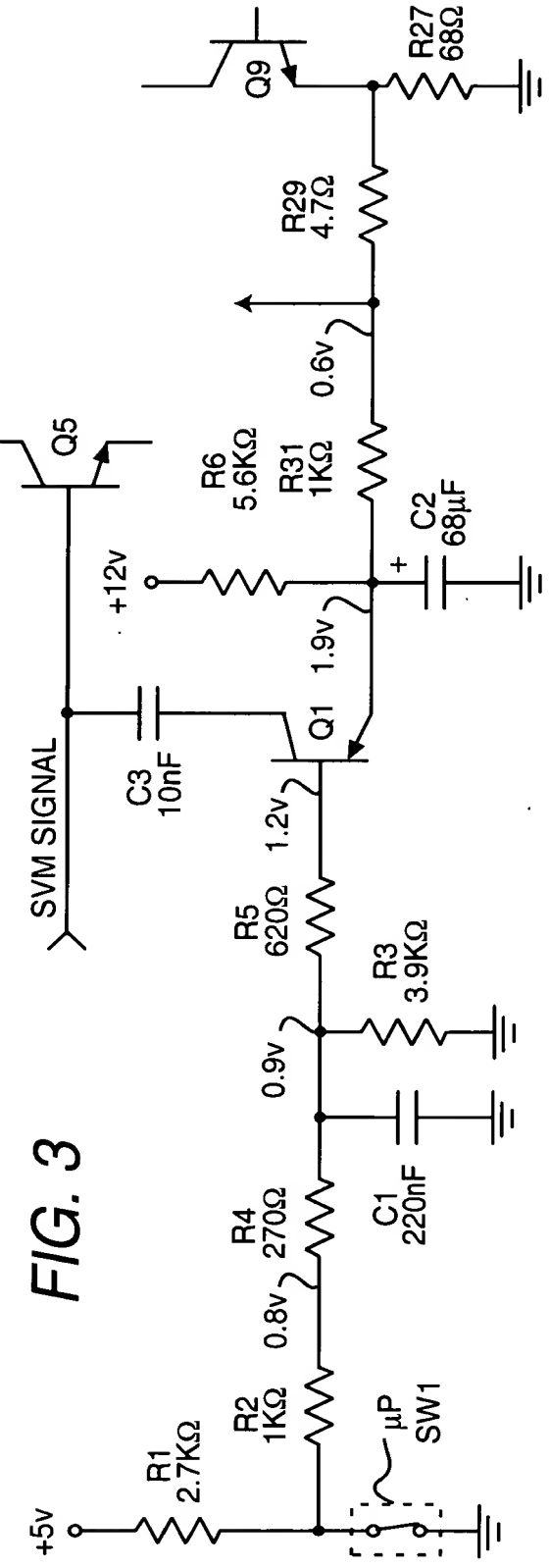


FIG. 3

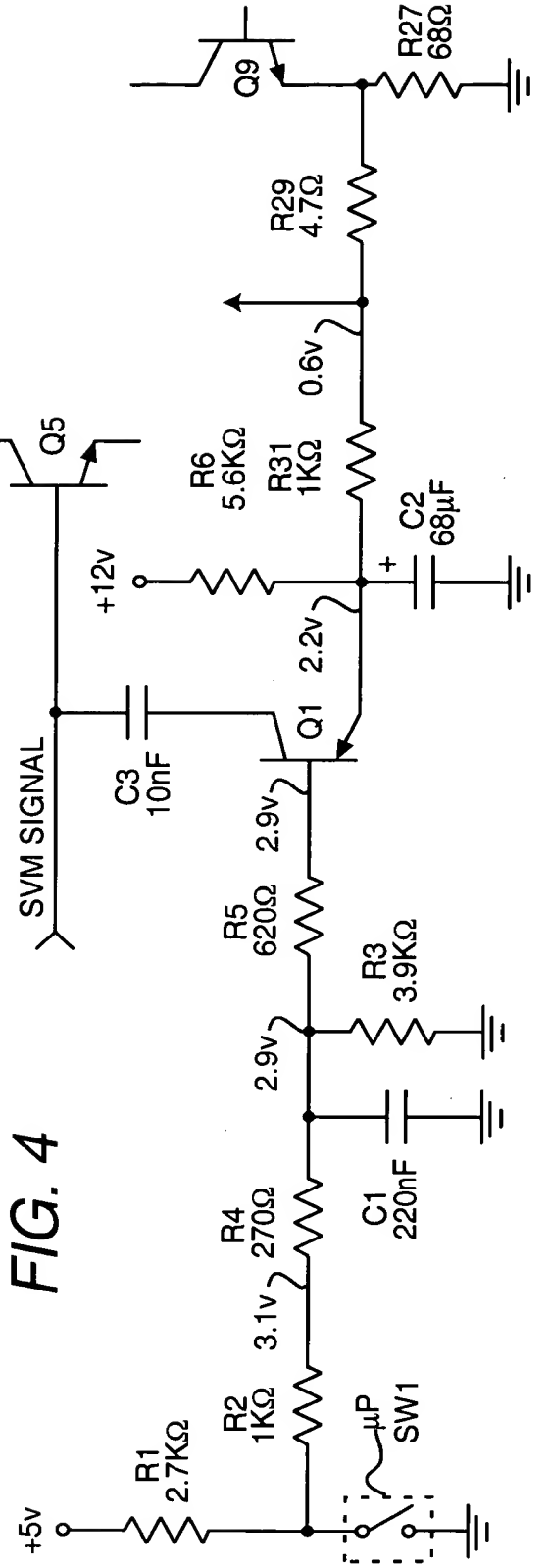


FIG. 4

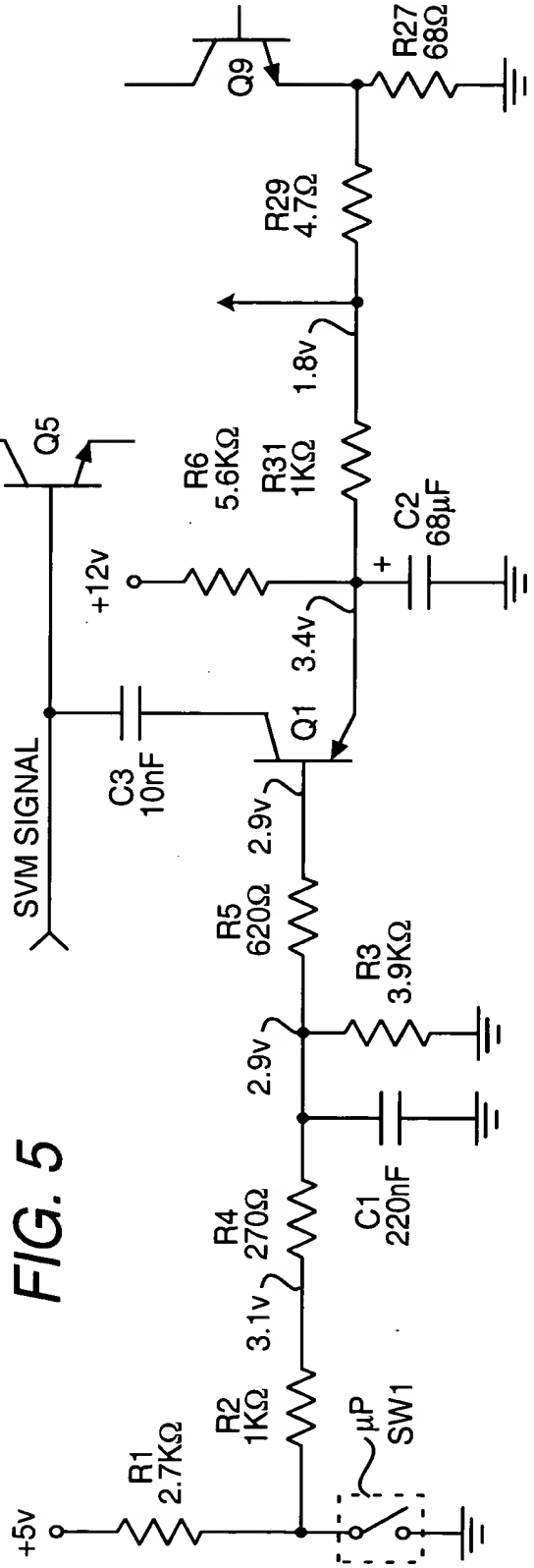


FIG. 5